REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 28-54 are in this case. Claims 31-33, 36, 37, 51 and 52 have been rejected under the judicially created doctrine of obviousness-type double patenting. Claims 28-54 have been rejected under § 112, second paragraph. Claims 28, 29, 35, 38-40, 46, 47, 49 and 53 have been rejected under § 102(e). Independent claims 28, 39 and 49 and dependent claims 29-38, 40, 41, 43, 44, 46-48 and 50-54 have been canceled. Dependent claims 42 and 45 have been amended. New independent claims 55-62 have been added.

Double Patenting Rejections

The Examiner has rejected claims 31-33, 36, 37, 51 and 52 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5, 12 and 13 of US Patent No. 6,243,787. The Examiner's rejection is respectfully traversed.

Claims 31-33, 36, 37, 51 and 52 now have been canceled, thereby rendering moot the Examiner's rejection of these claims.

§ 112, Second Paragraph Rejections

The Examiner has rejected claims 28-54 under § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, the Examiner has pointed out that the term "the host network interface" on the last lines of claims 28, 38 and 39 lacks antecedent basis and that the term "the network" on line 9 of claim 49 lacks antecedent basis. The remaining

claims have been rejected for depending from claims 28, 38 or 49. The Examiner's rejection is respectfully traversed.

Claims 28-41, 43, 44 and 46-54 have been canceled, thereby rendering moot the Examiner's rejection of these claims.

New independent claims 55-62 have been added. These claims are, respectively, claims 30, 34, 41, 43, 44, 48, 50 and 54, that were rejected only on § 112, second paragraph grounds, rewritten in independent form.

In new claims 55-60, the lack of antecedent basis for "the host network interface" has been resolved by changing "the host network interface" to "the host interface". Support for this amendment is found in the use of the terms "host interface" and "host network interface" interchangeably in the specification. See, for example, page 3 lines 15-27:

> In preferred embodiments of the present invention, a CPU and a peripheral device are linked to a packet- switching fabric by respective host and target network interfaces...In response to the interrupt, the target interface reads the interrupt cause from the peripheral device, and then sends a special interrupt package, including the interrupt cause, to the host interface. Preferably, the target interface sends the interrupt packet on the same channel as it sent the data packets, i.e., over the same "virtual lane" or route, and with the same priority as the data packets. It thus assures that the host interface will receive the interrupt packet only after it has received all of the preceding data packets. (emphasis added)

Also compare page 7 line 10:

> Bus 50 is coupled to fabric 26 by a host network interface unit 28. (emphasis added)

to page 9 lines 24-26:

> Fig. 3 is a flow chart that schematically illustrates a method by which data and accompanying interrupt packets are received and processed by host interface unit 28 and CPU 21, in accordance with a preferred embodiment of the present invention. (emphasis added)

In new claims 61 and 62, the lack of antecedent basis for "the network" has been resolved by changing "the network" to "the memory". Support for this amendment is found in the specification on page 8 lines 15-19:

> At a data writing step 60, device 25 writes data via bus 53 to TCA 42, to be conveyed by direct memory access to memory 22. The peripheral device assigns a priority to the data to be transmitted and informs the TCA of this priority. At a data sending step 62, the TCA packetizes the data and sends it over fabric 26 to the address of HCA 32, with the priority assigned by the peripheral device.

together with page 8 lines 25-28:

> When device 25 has finished posting to TCA 42 all of the data that it has to send, it asserts interrupt output 48, at an interrupt assertion step 64. At the same time, the peripheral device places the cause for the interrupt...in an interrupt cause register 49.

that show that the peripheral device asserts an interrupt signal after sending the data to the memory.

Correspondingly, claim 42 has been amended to depend from claim 57 and claim 45 has been amended to depend from claim 59. With new independent claims 57 and 59 allowable in their present form, it follows that claims 42 and 45, that depend therefrom, also are allowable.

§ 102(e) Rejections – Bailey et al. '573

The Examiner has rejected claims 28, 29, 35, 38-40, 46, 47, 49 and 53 under § 102(e) as being anticipated by Bailey et al., US Patent No. 6,295,573. The Examiner's rejection is respectfully traversed.

Claims 28, 29, 35, 38-40, 46, 47, 49 and 53 have been canceled, thereby rendering moot the Examiner's rejection of these claims.

In view of the above amendments and remarks it is respectfully submitted that independent claims 55-62, and hence dependent claims 42 and 45 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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